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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,212	02/07/2002	Anshuman Nayak	ACCEL-P001	2745

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EXAMINER	
WOOD, WILLIAM H	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,212	NAYAK ET AL.	
	Examiner	Art Unit	
	William H. Wood	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-52* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

TR HL

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1 and 21-39, drawn to a computer-automated method for electronic design specification comprising specifying at least one resource or functionality using at least one construct in a Resource Description Language (RDL) wherein at least one component or function is specifiable for processing by a high-level synthesis compiler, classified in class 717, subclass 104.

II. Claim 2, drawn to computer-automated method for electronic design specification comprising specifying an interface of a component in a language-independent manner, wherein a compiler may infer functionality therefrom, classified in class 717, subclass 104.

III. Claim 3, drawn to A computer-automated method for electronic design specification comprising the step of specifying an interface of a component in a language-independent manner, wherein a synthesis compiler automatically processes a component cycle-by-cycle timing behavior without having to specify explicitly a timing diagram for the component, classified in class 717, subclass 104.

IV. Claim 4, drawn to A computer-automated method for electronic design specification comprising the step of specifying an interface of a component

in a language-independent manner, wherein a synthesis compiler processes a component cycle-by-cycle timing behavior, the component having a fixed latency, classified in class 717, subclass 104.

V. Claim 5, drawn to A computer-automated method for electronic design specification comprising the step of specifying an interface of a component in a language-independent manner, wherein a synthesis compiler processes a component cycle-by-cycle timing behavior, the component having a variable latency, classified in class 717, subclass 104.

VI. Claim 6, drawn to A computer-automated method for electronic design specification comprising the step of specifying an interface of a component in a language-independent manner, wherein a synthesis compiler processes a component cycle-by-cycle timing behavior, the component having a pipeline implementation, classified in class 717, subclass 104.

VII. Claim 7, drawn to A computer-automated method for electronic design specification comprising the step of specifying an interface of a component in a language-independent manner, wherein a synthesis compiler processes a component cycle-by-cycle timing behavior, the component having a non-pipeline implementation, classified in class 717, subclass 104.

VIII. Claim 8, drawn to A computer-automated method for electronic design specification comprising the step of specifying an interface of a component in a language-independent manner, wherein a synthesis compiler

processes a component cycle-by-cycle timing behavior, the component having a synchronous interface, classified in class 717, subclass 104.

IX. Claim 9, drawn to A computer-automated method for electronic design specification comprising the step of specifying an interface of a component in a language-independent manner, wherein a synthesis compiler processes a component cycle-by-cycle timing behavior, the component having an asynchronous interface, classified in class 717, subclass 104.

X. Claim 10, drawn to A computer-automated method for electronic design specification comprising the step of specifying an interface of at least one Intellectual-Property (IP) core in a language-independent manner, wherein a synthesis compiler infers the IP core functionality automatically to instantiate a corresponding IP core, classified in class 717, subclass 104.

XI. Claim 11, drawn to A computer-automated method for electronic design specification comprising the step of specifying an interface of a class of Intellectual-Property (IP) cores with one description in a language-independent manner, wherein a synthesis compiler infers an actual IP core to be used automatically and generates a true interface automatically, classified in class 717, subclass 104.

XII. Claim 12, drawn to A computer-automated method for electronic design specification comprising the step of specifying a timing interface of at least one Intellectual-Property (IP) core without use of a timing diagram of such IP-core in a language-independent manner, wherein a synthesis compiler

infers an IP-core timing behavior for synthesizing an application in which the IP-core is used, classified in class 717, subclass 104.

XIII. Claim 13, drawn to A computer-automated method for electronic design specification comprising the step of inferring a floorplan of a final hardware on silicon from a generic description stored with one or more Intellectual Property (IP) cores and controlled by a user based on an application for which hardware is being generated, classified in class 717, subclass 104.

XIV. Claim 14, drawn to A computer-automated method for electronic design specification comprising the step of specifying a function block in a language-independent manner, wherein a synthesis compiler infers a functionality of the function block, classified in class 717, subclass 104.

XV. Claim 15, drawn to A computer-automated method for electronic design specification comprising the step of specifying a timing interface of a function block without using a timing diagram of the function block in a language-independent manner, wherein a synthesis compiler infers a timing behavior of the function block for synthesizing an application in which the function block may be used, classified in class 717, subclass 104.

XVI. Claim 16, drawn to A computer-automated method for electronic design specification comprising the step of specifying a virtual function block comprising one or more function block or Intellectual Property (IP) core,

wherein a synthesis compiler infers a functionality of the virtual function block, classified in class 717, subclass 104.

XVII. Claim 17, drawn to A computer-automated method for electronic design specification comprising the step of specifying a timing interface of a virtual function without using a timing diagram of a function block, wherein a synthesis compiler infers a timing behavior of the virtual function for synthesizing an application in which the virtual function may be used, classified in class 717, subclass 104.

XVIII. Claim 18, drawn to A computer-automated method for electronic design specification comprising the step of specifying a database to store one or more characteristic of an Intellectual Property (IP) core which may be queried by the an RDL specification of the IP core to return information about the IP core, classified in class 717, subclass 104.

XIX. Claim 19, drawn to A computer-automated method for electronic design comprising the step of generating a hierarchical graph representing one or more required resource requirement of one or more computational block in an application being synthesized, classified in class 717, subclass 104.

XX. Claim 20, drawn to A computer-automated method for electronic design comprising the step of identifying and matching a functionality of a computation block in an application with that of a function block, a virtual function or an Intellectual Property (IP) core to instantiate the computation block, classified in class 717, subclass 104.

XXI. Claim 40, drawn to A computer-automated method for electronic design comprising the step of generating a hierarchical graph representing a resource target and an interface, classified in class 717, subclass 104.

XXII. Claim 41, drawn to A computer-automated method for electronic design comprising the step of generating a signature of a functionality graph such that the signature is unique, classified in class 717, subclass 104.

XXIII. Claim 42, drawn to A computer-automated method for electronic design comprising the step of generating a signature of a resource graph such that the signature is unique, classified in class 717, subclass 104.

XXIV. Claims 43 and 47, drawn to A computer-automated method for electronic design comprising the step of graph-matching to map a functionality block on an optimally-suited resource graph, classified in class 717, subclass 104.

XXVI. Claim 44, drawn to A computer-automated method for electronic design comprising the step of generating an interface block to enable invocation of a function block for synthesizing an application to a target, classified in class 717, subclass 104.

XXVII. Claim 45, drawn to A computer-automated method for electronic design specification comprising the step of creating a table structure; and populating the table structure with one or more function flow block or Intellectual Property (IP) core, wherein the function block or IP-core area,

performance, or interface characteristics comprise one ore more capture, classified in class 717, subclass 104.

XXVIII. Claim 46, drawn to A computer-automated method for electronic design comprising the step of querying a table structure to obtain an area or performance characteristic of an IP-core or function block optimally to map such area or performance characteristic to one or more resource, classified in class 717, subclass 104.

XXIX. Claim 48, drawn to A computer-automated method for electronic design specification comprising the step of specifying and querying an interface or characteristic of an Intellectual Property (IP) core for a Field Programmable Gate Array (FPGA) generator according substantially to a Xilinx vendor format and specification to incorporate in a synthesized design on a target, classified in class 717, subclass 104.

XXX. Claim 49, drawn to A computer-automated method for electronic design specification comprising the step of specifying and querying an interface or characteristic of an Intellectual Property (IP) core for a digital signal professor (DSP) builder according substantially to an Altera vendor format and specification to incorporate in a synthesized design on a target, classified in class 717, subclass 104.

XXXI. Claim 50, drawn to A computer-automated method for electronic design specification comprising the step of specifying and querying an interface and characteristic of an Intellectual Property (IP) core for a tool according

substantially to a Quicklogic format and specification to incorporate in a synthesized design on a target, classified in class 717, subclass 104.

XXXII. Claim 51, drawn to A computer-automated method for electronic design specification comprising the step of specifying and querying an interface and the characteristics of an Intellectual Property (IP) core from a soft core vendor for use in an Application Specific Integrated Circuit (ASIC) or Field Programmable Gate Array (FPGA) architecture, classified in class 717, subclass 104.

XXXIII.Claim 52, drawn to A computer-automated method to synthesize an application to a target comprising the steps of reading and parsing a resource description language (RDL) description of a target; generating an RDL Abstract Syntax Tree; generating a resource graph for the target; generating a functionality graph from an application; generating a signature of one or more node of the functionality graph; querying an architecture interface of the resource graph; generating one or more signature of a functionality of the node in the resource graph; optimally matching one or more signature of the node of the functionality and resource graphs to map optimally a function to a resource of the target; and generating an interface in a synthesized application to invoke one or more function block, Intellectual Property core (IP-core), or component on the target, classified in class 717, subclass 104.

Inventions I through XXXIII are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, inventions I-XXXIII have separate utility as indicated individually by their specific and separate method steps repeated above for clarity. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and the searchs required for Groups I-XXXIII are not required for the other Groups I-XXXIII, restriction for examination purposes as indicated is proper.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William H. Wood whose telephone number is (571)-272-3736. The examiner can normally be reached 9:00am - 5:30pm Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571)-272-3719. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

William H. Wood
June 27, 2005

ANIL KHATRI
PRIMARY EXAMINER